

General Description

The QM02N65U is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The QM02N65U meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	2	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	1.3	A
I_{DM}	Pulsed Drain Current ²	4	A
EAS	Single Pulse Avalanche Energy ³	16	mJ
I_{AS}	Avalanche Current	3.4	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	40	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3	$^\circ C/W$

Product Summary

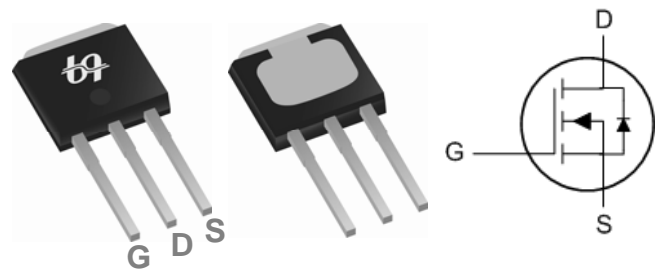


BVDSS	RDSON	ID
650V	8 Ω	2A

Applications

- High efficient switched mode power supplies
- Electronic lamp ballast
- LED Lighting
- Adapter/charger

TO251 Pin Configuration



Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.37	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=1A$	---	6.3	8	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2		5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-43	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=10V, I_D=1A$	---	1.7	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=60V, V_{GS}=10V, I_D=1A$	---	5.3	---	nC
Q_{gs}	Gate-Source Charge		---	1.44	---	
Q_{gd}	Gate-Drain Charge		---	1.42	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=300V, V_{GS}=10V, R_G=10\Omega, I_D=1A$	---	18	---	ns
T_r	Rise Time		---	12	---	
$T_{d(off)}$	Turn-Off Delay Time		---	25	---	
T_f	Fall Time		---	14	---	
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, F=1\text{MHz}$	---	290	---	pF
C_{oss}	Output Capacitance		---	25	---	
C_{rss}	Reverse Transfer Capacitance		---	4	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=50V, L=1\text{mH}, I_{AS}=1.5A$	3.2	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	2	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	4	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=50V, V_{GS}=10V, L=1\text{mH}, I_{AS}=1.5A$
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

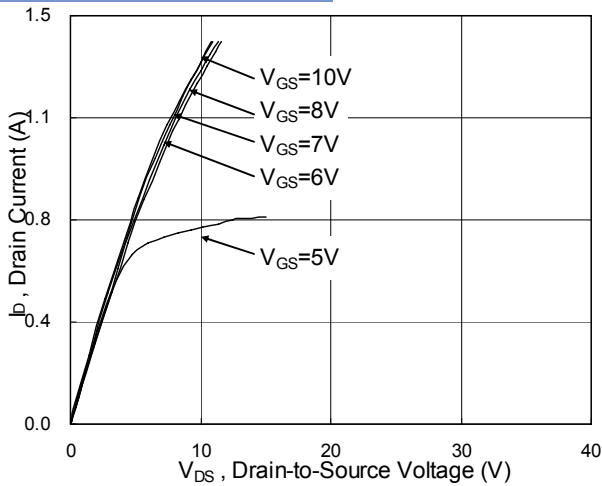


Fig.1 Typical Output Characteristics

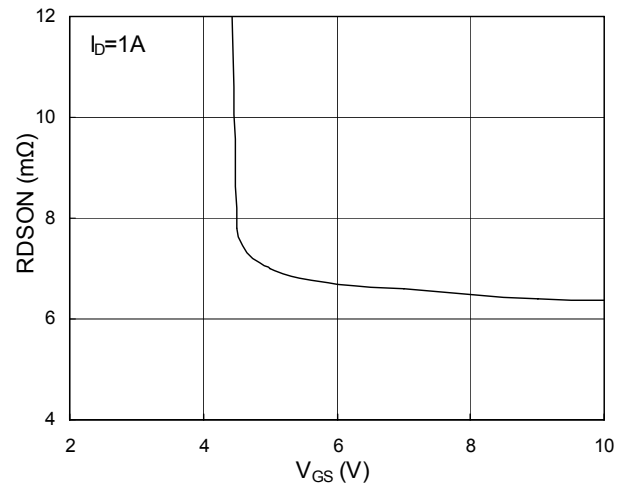


Fig.2 On-Resistance vs. G-S Voltage

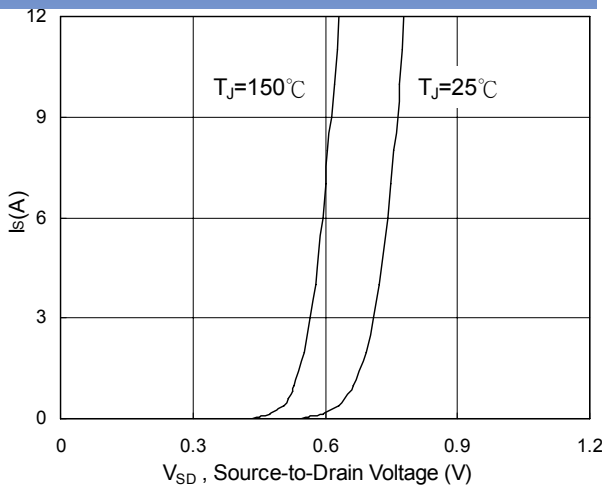


Fig.3 Forward Characteristics of Reverse

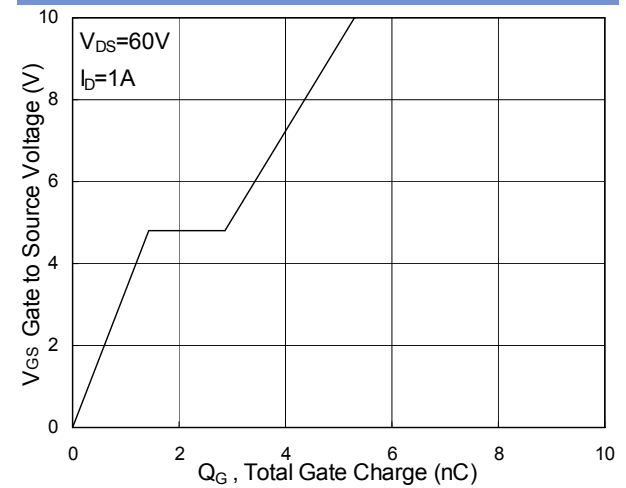


Fig.4 Gate-charge Characteristics

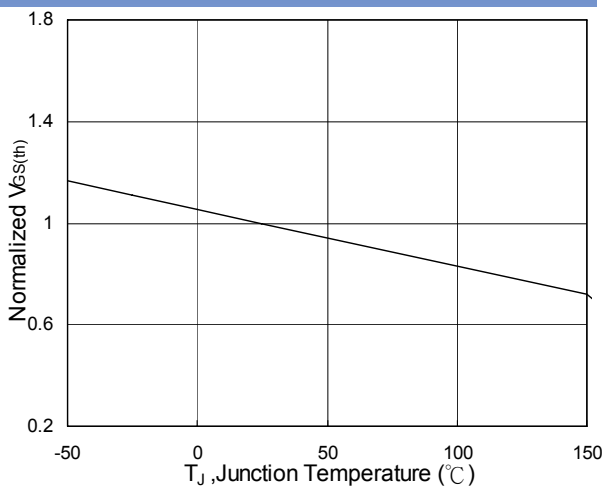


Fig.5 $V_{GS(th)}$ vs. T_J

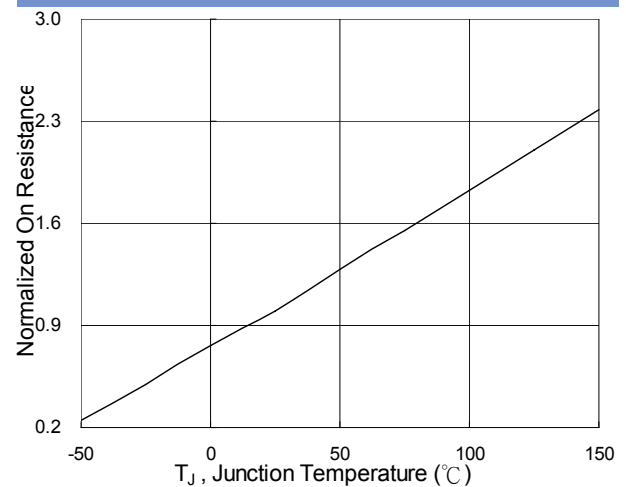


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

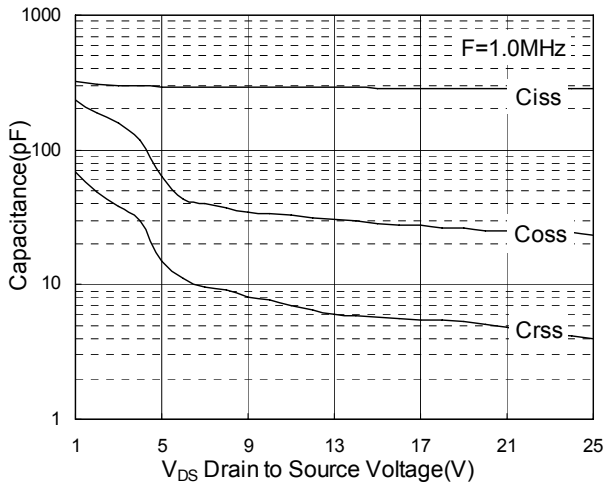


Fig.7 Capacitance

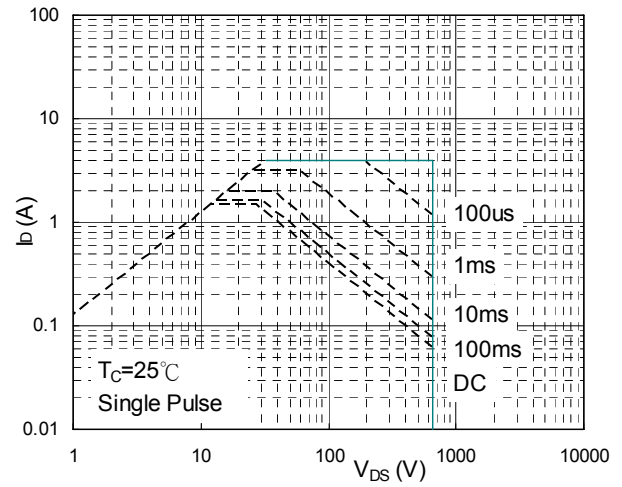


Fig.8 Safe Operating Area

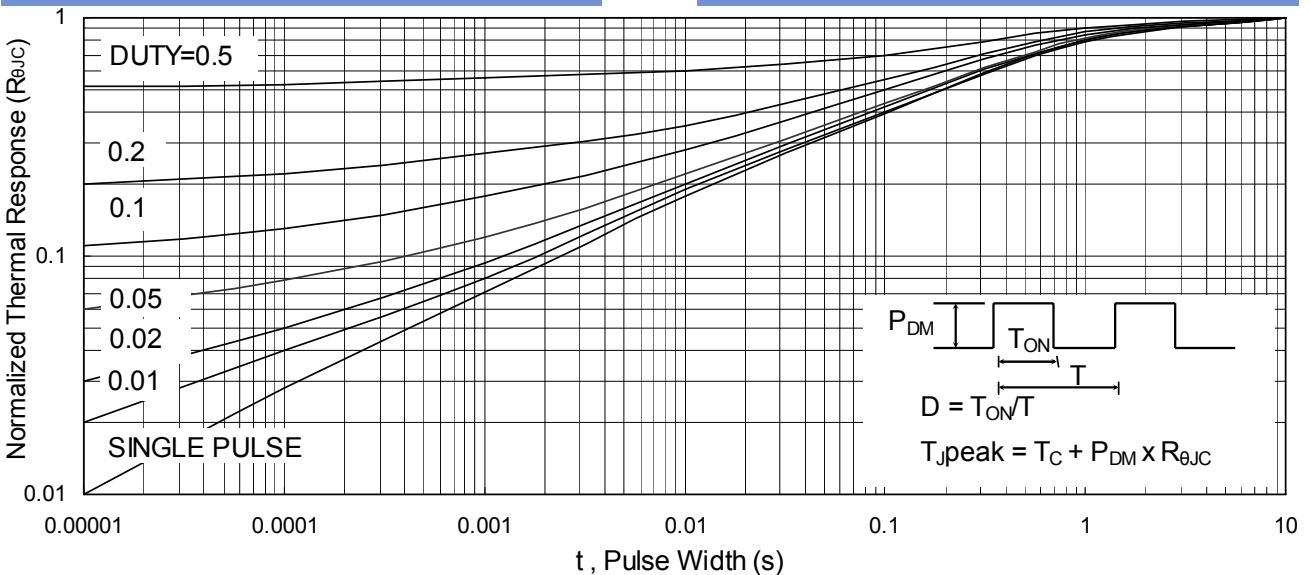


Fig.9 Normalized Maximum Transient Thermal Impedance

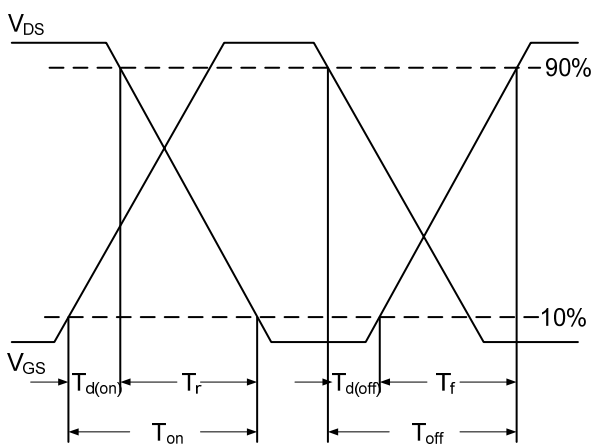


Fig.10 Switching Time Waveform

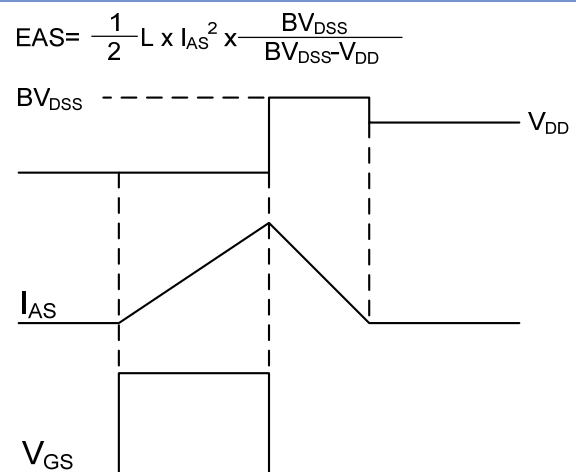


Fig.11 Unclamped Inductive Switching Wave