

General Description

The QM03N65D is the highest performance N-ch MOSFETs with specialized high voltage technology, which provide excellent RDSON and gate charge for most of the SPS, Charger ,Adapter and lighting applications .

The QM03N65D meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

Features

- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	1.9	A
I_{DM}	Pulsed Drain Current ²	6	A
EAS	Single Pulse Avalanche Energy ³	26.2	mJ
I_{AS}	Avalanche Current	7	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	90	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.4	$^\circ C/W$

Product Summary

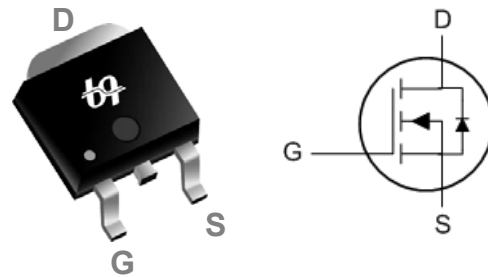


BVDSS	RDSON	ID
650V	4 Ω	3A

Applications

- High efficient switched mode power supplies
- LED Lighting
- LCD TV/ Monitor
- Adapter

TO252 Pin Configuration



Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.63	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=1.5A$	---	3.2	4	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2	---	5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-7.52	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=520V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	2	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=10V, I_D=1.5A$	---	3	---	S
Q_g	Total Gate Charge (10V)	$V_{DS}=520V, V_{GS}=10V, I_D=1A$	---	12.6	---	nC
Q_{gs}	Gate-Source Charge		---	3.84	---	
Q_{gd}	Gate-Drain Charge		---	3.97	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=300V, V_{GS}=10V, R_G=10\Omega, I_D=1A$	---	7.4	---	ns
T_r	Rise Time		---	18.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	18.4	---	
T_f	Fall Time		---	24.8	---	
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, F=1\text{MHz}$	---	490	---	pF
C_{oss}	Output Capacitance		---	38.5	---	
C_{rss}	Reverse Transfer Capacitance		---	4.6	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=50V, L=1\text{mH}, I_{AS}=3.5A$	6.6	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	3	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=1A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	168	---	nS
Q_{rr}	Reverse Recovery Charge		---	482	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=50V, V_{GS}=10V, L=1\text{mH}, I_{AS}=7A$
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

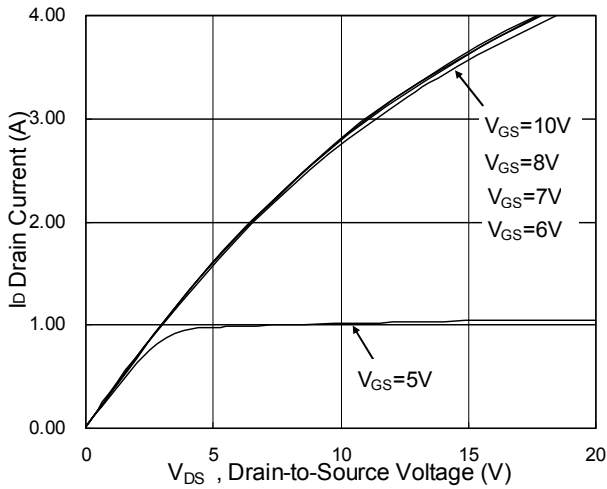


Fig.1 Typical Output Characteristics

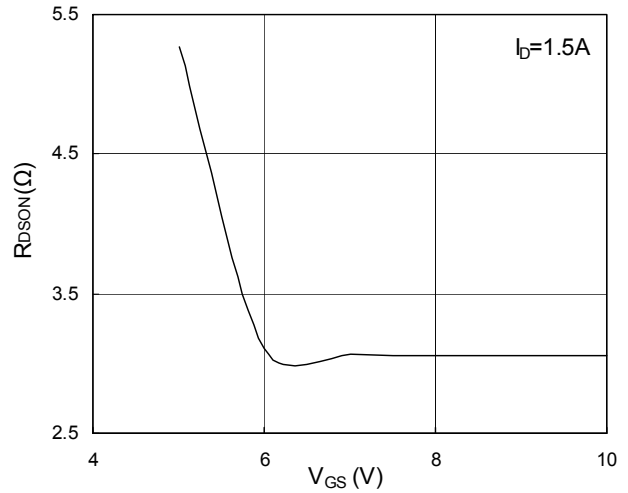


Fig.2 On-Resistance vs. G-S Voltage

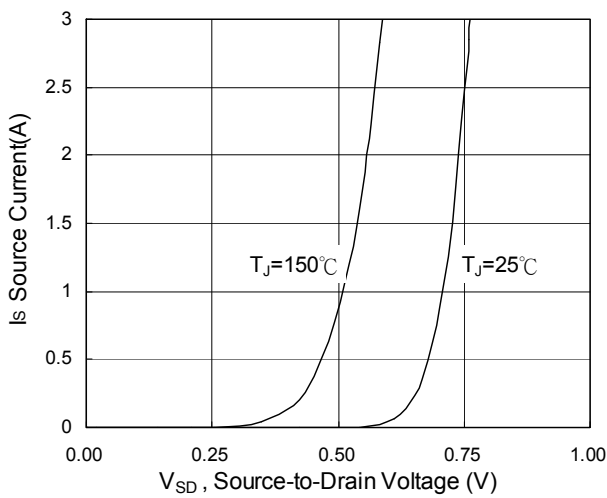


Fig.3 Forward Characteristics of Reverse

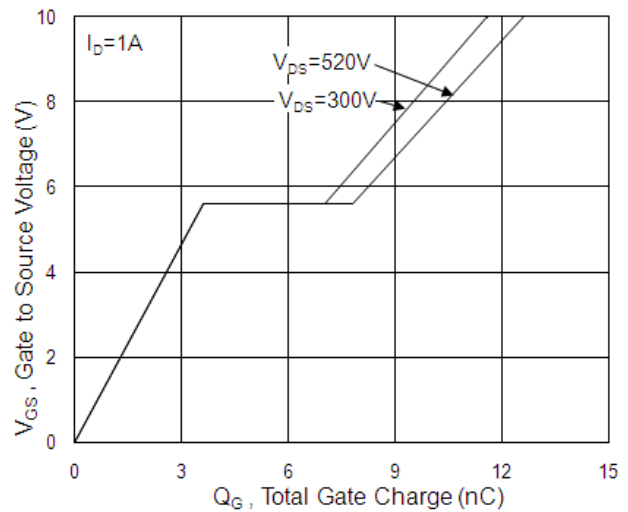


Fig.4 Gate-Charge Characteristics

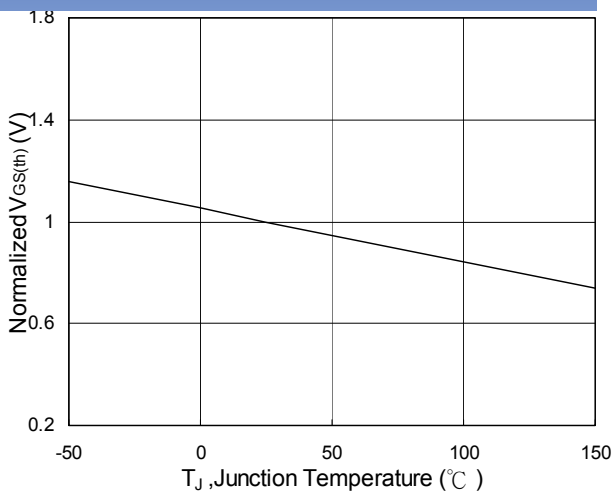


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

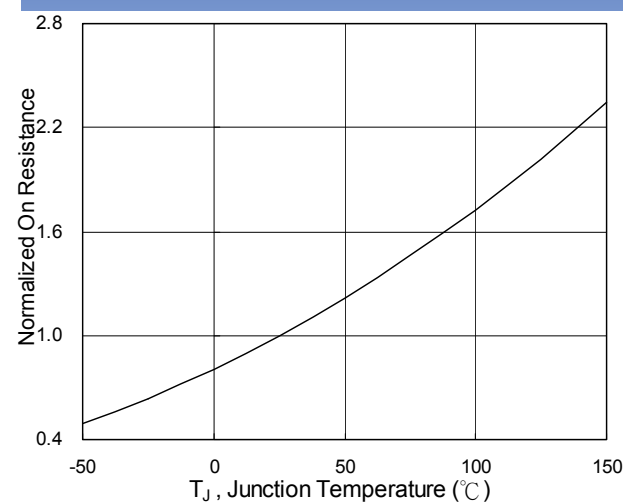


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

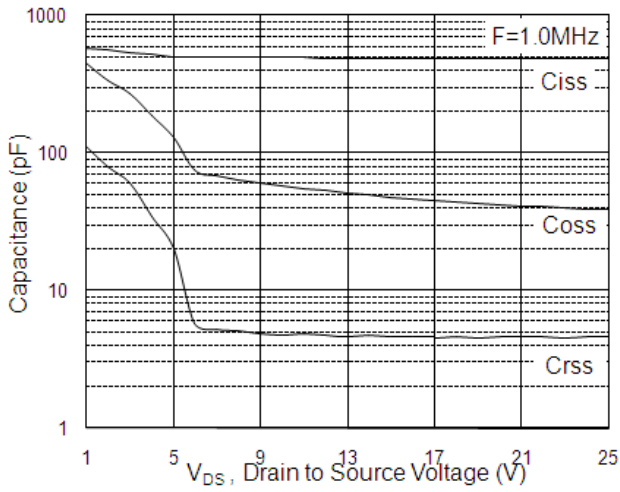


Fig.7 Capacitance

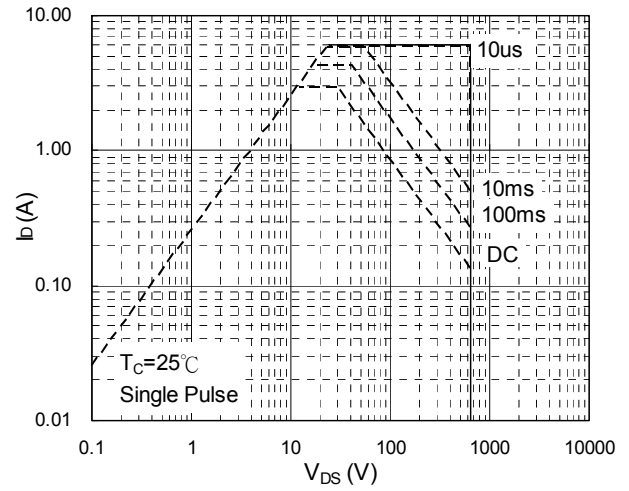


Fig.8 Safe Operating Area

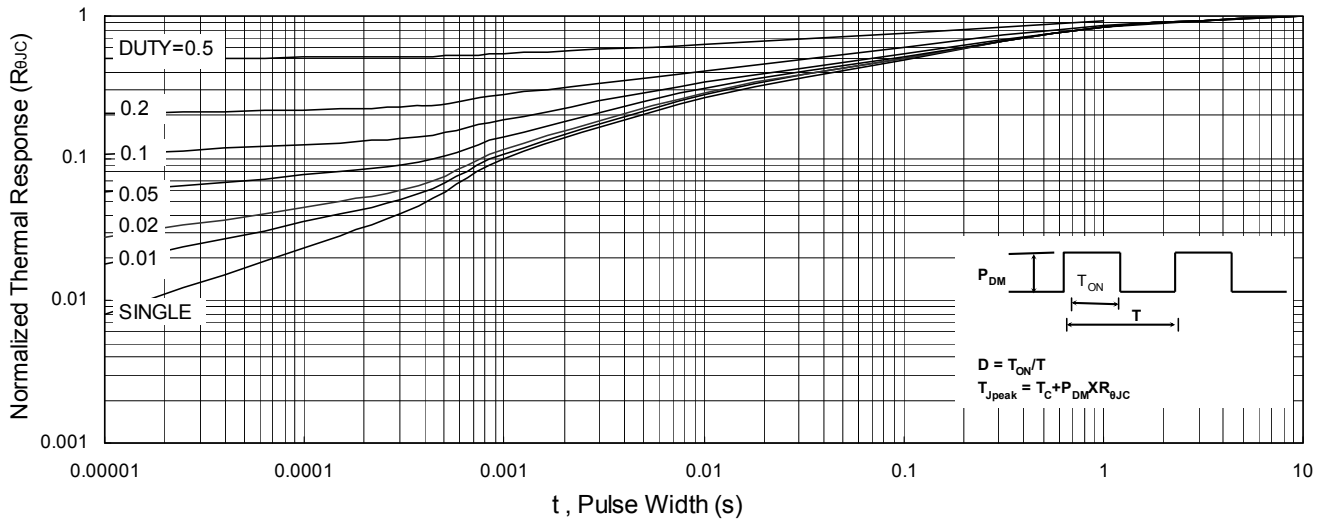


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform